Relaxation Oscillator Using Closed-loop Dual Comparator for Biomedical Applications

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Submission date: 15-Mar-2022 11:48AM (UTC+0700) Submission ID: 1784647787 File name: sing_Closed-loop_Dual_Comparator_for_Biomedical_Applications.pdf (9.35M) Word count: 3177 Character count: 17266

Relaxation Oscillator Using Closed-loop Dual Comparator for Biomedical Applications

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Abstract- People's rising concerns about health have fueled research into high-performance biomedical devices and circuits, such as sensors and implantable systems on a chip. It is important for these biomedical devices to operate at the same low frequency to treat certain organs and diseases. Thus, the clock generator needs to be able to provide low frequency clock pulses with minimal size and high reliability. These constraints elevate power consumption and production cost within the circuit design to key parameters. One promising candidate is relaxation oscillator which has good on-chip compatibility, and superior frequency stability. This paper proposes a novel relaxation oscillator using closed-loop dual comparator. A frequency in the band of 50Hz to 2.5kHz can be generated by replacing the value of resistors and capacitor in all possible combinations. The simulation and experimental result confirm that closed-loop dual comparator-based relaxation oscillator provides low frequency with lower cost and more simplicity due to fewer components.

Keywords— relaxation oscillator, 555 timer IC, comparator, square wave generator.

I. INTRODUCTION

Through the years, a variety of oscillators have emerged, each of them delivers unique advantages with different tradeoffs. Many works reported from a wide range of complexity to fulfill the need of future applications such as smart devices, wearable electronics, biomedical devices, IoT, and many more [1]-[3]. The increasing concerns on health recently have governed interest in the research of implantable and biomedical devices which operate at low frequency to match the frequency of human body. Thus, an oscillator with long-term reliable operation, minimal power consumption, and compact size is in great demand [4], [5].

Amongst many methods of reference clock generation, relaxation oscillator is the most popular candidate for low frequency and low power oscillator. The properties of 7 axation oscillators such as large tuning ranges and 8 nperature-stable operation facilitating on-chip integration 7 take it suitable to use at lower frequencies. Compared to 7 g oscillators, relaxation oscillators can offer superior frequency stability, linear control, wide tuning range, and high power efficiency [6]-[8]. Hence, relaxation oscillator has great potential and attractive to be used as nextgeneration low-cost solution for biomedical applications.

One of the distinguished relaxation oscillators in history is the 555 timer oscillator. As can be seen in Fig. 1, this relaxation oscillator comprised of: a resistive voltage divider

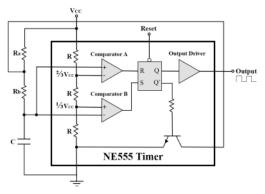


Fig. 1. Block diagram of the 555 Timer Oscillator [9].

2) at sets the voltage at the inverting input of comparator A at 2/3Vcc and the non-inverting input of comparator B at 1/3Vcc; two comparators which produce an output voltage dependent upon the volta 2 difference at their inputs; an SR flip-flop which produces HIGH or LOW output at Q based 4 the comparator's two outputs; and a discharge transistor connected to the output Q' of SR flip-flop [10].

It is interesting to see how each of these main functional elements work together to generate a square wave with an adjustable period and duty cycle determined by an externally adjusted RC time constant [11]. Whenever a comparator's non-inverting input is above its inverting input, the comparator's output is HIGH and vice versa. Comparator A's a tput drives the Reset (R) input of the flip-flop, meanwhile comparator B's output drives the Set (S) input of the flipflop. The HIGH and LOW pulses generated are due to the constantly Set and Reset flip-flop [12]. The philosophy of the 555 timer oscillator is that square waves signal can be generated due to the function of SR flip-flop with an additional discharge transistor to enable periodic square wave operation.

This paper proposes the elimination of discharge transistor and SR flip flop by means of functioning the two comparators to 'Set' and 'Reset' each other to produce periodic square waveform. The term closed-loop dual comparator is introduced to describe this interconnection. As a result, lower power consumption and lower cost production of a low frequency oscillator can be realized with fewer components for biomedical applications.

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II. BACKGROUND

Fig. 2(a) reveals the relaxation oscillator circuit using s closed-loop dual comparator. As can be seen, the two comparators interconnection is utilized to replace the role of SR flip-flop which toggle the output HIGH and LOW alternately, and the role of discharge transistor which provide a path for capacitor discharge to ground. The oscillation principle of the proposed closed-loop dual comparator is based on the alternating charging and discharging of the capacitor C controlled by the output voltage of comparator A. The capacitor voltage as a function of time can be defined as

$$V_C(t) = V_{final} - (V_{final} - V_{initial})e^{-t/R_a C}$$
(1)

The output voltage of comparator A is dependent upon the voltage difference at its inputs, which is controlled by comparator B via the feedback network. If the output of comparator B is HIGH, the output of comparator A will also be high, and vice versa. Comparator B will produce HIGH output whenever the capacitor voltage is below 1/3VCC, and LOW output whenever the capacitor voltage is above 1/3 VCC. However, due to the nonidealities of the comparators, the output will not change immediately. Fig. 2(c) depicts the minimum voltage V_{TRIP} needed for the comparators to detect the difference between their inputs. When the capacitor voltage reaches its peak at VREF + VTRIP, the output of comparator B flips to LOW, discharging the capacitor through Ra to the ground of comparator A. Consequently, the capacitor voltage falls to VREF - VTRIP, thus the output of comparator B flips to HIGH, charging the capacitor through Ra. Hence, the time when the output pulse is HIGH (T1) can be obtained from (1) by setting $V_{C}(T1) = 1/3V_{CC} + V_{TRIP}$, namely,

$$T_1 = ln\left(\frac{2/3V_{CC} + V_{TRIP}}{2/3V_{CC} - V_{TRIP}}\right) R_a C \tag{2}$$

The time when the output pulse is LOW (T2) can be obtained from (1) by setting $V_C(T2) = 1/3 V_{CC} - V_{TRIP}$.

$$T_2 = ln\left(\frac{1/3V_{CC} + V_{TRIP}}{1/3V_{CC} - V_{TRIP}}\right) R_a C \tag{3}$$

V_{TRIP} can be obtained by finding the resolution of the comparators. As can be seen from (2), if V_{TRIP} approaches 2 ro, comparator B will flip instantly and there will be no time for the capacitor to charge and discharge, causing the pulse width (T1) to approach zero. Moreover, the duty cycle is also determined by the ratio of V_{REF} in the non-inverting input of comparator B to V_{CC}. Thus, the circuit in Fig. 2(a) which uses three identical resistors R as voltage divider has a 33% duty cycle. A lower frequency can be achieved by increasing the value of time constant R_aC with consideration of the comparator resolution.

Double reference is not required as the circuit can still work if the middle resistor is eliminated, thus the inverting input of comparator A and the non-inverting input of comparator B share a common voltage reference determined in (4). Therefore, further improvement can be made by simplifying the circuit to single reference as illustrated in Fig. 2(b), which comprised of only one internal resistor R and one external resistor Rb as the voltage divider networks.

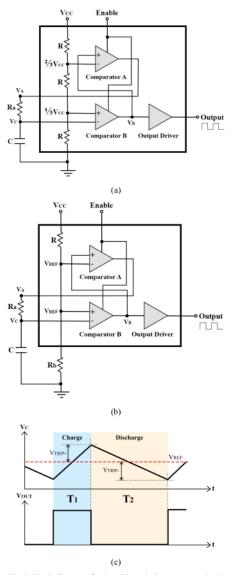


Fig. 2. Block diagram of a closed-loop dual comparator circuit configured as a free-running oscillator. (a) Double reference circuit. (b) Single reference circuit. (c) Voltage trip on the comparators.

$$V_{REF} = \frac{R_b}{R + R_b} V_{CC} \tag{4}$$

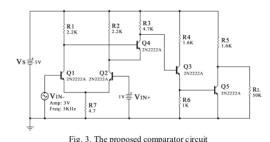
$$T_1 = \ln\left(\frac{V_{CC} - V_{REF} + V_{TRIP}}{V_{CC} - V_{REF} - V_{TRIP}}\right) R_a C \tag{5}$$

$$T_2 = \ln\left(\frac{V_{REF} + V_{TRIP}}{V_{REF} - V_{TRIP}}\right) R_a C \tag{6}$$

The duty cycle is determined by the ratio of Rb/(R+Rb) and when R = Rb we have T1 = T2 and the output waveform has a 50% duty cycle.

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Fig. 3 reveals the architecture of the proposed comparator. It consists of only five transistors. The sing ation result of the proposed comparator is shown in Fig. 4. When the inverting input voltage is higher than the noninverting input voltage, the output is LOW. When the noninverting input is higher than the inverting input, the output switches to HIGH. Hence, the proposed relaxation oscillator can be implemented using a total of 10 transistors, and 15 resistors. Compared to the 555 timer oscillator which composed of 23 transistors, 15 resistors, and 2 diodes [13], a relaxation oscillator using a closed-loop dual comparator is more than twice simpler. With minimal components, the proposed relaxation oscillator can be realized with lower manufacturing costs.



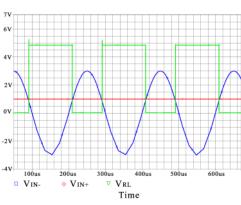


Fig. 4. The simulation results of the proposed comparator circuit in figure 3.

III. SIMULATION AND EXPERIMENTAL RESULTS

For simulation purposes, the closed-loop dual comparator is im semented using LM393 and a single supply voltage of 3V. Fig. 5 demonstrates the operation waveforms of the proposed closed-loop dual comparator circuit shown in Fig. 2(b) in start-up and steady-state conditions based on PSPICE simulation results. At start-up condition depicted in Fig. 5(a), at t = T0, the voltage across the capacitor C starts with zero. Because energy cannot be changed instantaneously, the charging capacitor voltage needs time to rise to V_{REF} . The higher the time constant and the VREF level, the longer the period of oscillation and start-up condition. During the startup condition, the non-inverting input of comparator B is lower than the inverting input. Thus, comparator B starts with HIGH output state, and so does comparator A. The HIGH output voltage of comparator A charges the capacitor until it reaches V_{REF} at t = T1, and the oscillation starts.

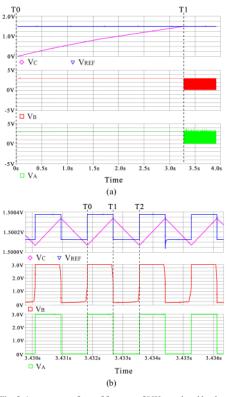


Fig. 5. A square waveform of frequency 580Hz produced by the closed-loop dual comparator circuit in Fig. 2(b) using LM393. (a) Start-up condition. (b) Steady state.

At steady-state operation which can be observed from Fig. 5(b), at t = T1 the output of comparator B change state to LOW after it detects $V_{\rm C}$ is above $V_{\rm REF}$ after a minimum voltage difference of $V_{\rm TRP}.$ At t = T2, the output of comparator B flips to HIGH after it detects $V_{\rm C}$ falls below $V_{\rm REF},$ and the cycle repeats. PSPICE simulation results confirm that with Ra = 470k\Omega and C = 10uF, the circuit can generate about 580Hz frequency of oscillations. The output of comparator A and B are in phase, and comparator A generates better square waves than comparator B, thus the output of comparator A is chosen as the output oscillation.

To lower the output frequency, the resistor Ra and capacitor C can be adjusted to higher values while considering the comparator specification. According to the simulation results shown in Table I, the closed-loop dual

TABLE I. SUMMARY OF SIMULATION RESULTS

Parameter	Frequency	Startup Time	Duty Cycle	Power Consumption
$Ra = 470k\Omega$, C = 22uF	52.85Hz	1.10s	10%	1.05mW
$Ra = 470k\Omega$, C = 22uF	178.27Hz	4.24s	33%	lmW
$Ra = 470k\Omega$, C = 10uF	225,92Hz	1.06s	20%	0.75mW
$Ra = 470k\Omega$, C = 10uF	578.84Hz	3.27s	50%	0.86mW
$Ra = 100k\Omega$, C = 10uF	2.41kHz	0.76s	50%	0.65mW

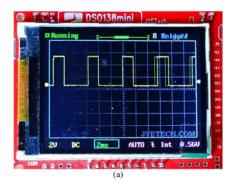
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comparator circuit can produce frequency in the band of 50Hz to 2.5kHz. Also, the proposed relaxation oscillator can perform various duty cycle by simply changing the resistor Rb value. Changing the duty cycle can result in different frequencies of oscillation, even though the RC value is the same. As can be seen from the simulation results, the power consumption of the proposed closed-loop dual comparator circuit is within milliwatts power, by using IC LM393. The lower the frequency of oscillations, the lesser the power consumption.

The proposed closed-loop dual comparator circuit of Fig. 2(a) and Fig. 2(b) is straightforwardly verified by the experimental result, as shown in Fig. 6 using LM393 and the parameters shown in Table II for low frequency operation.

TABLE II.	PARAMETERS OF THE CLOSED-LOOP DUAL	
COMPARAT	R CIRCUIT IN FIG. 2(A) AND FIG. 2(B).	

	Parameters		
Components	Double Reference	Single Reference	
Voltage source V _{CC}	5 V dc	5 V de	
Output frequency f (calculated)	370 Hz	415 Hz	
Comparator A and B	LM393	LM393	
Internal resistor R	10 kΩ	10 kΩ	
Resistor to adjust time constant Ra	1 MΩ	1 MΩ	
Resistor as voltage divider Rb	-	10 kΩ	
Capacitor C	0.47 uF	0.47 uF	
Duty cycle D	33.33%	50%	



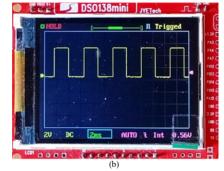


Fig. 6. Experim**cit**al results of the closed-loop dual comparator circuit using LM393 and single supply voltage +5V. (a) Double reference circuit. (b) Single reference circuit.

The measured frequency based on the experiment result in Fig. 6(a) and Fig 6(b) is 180Hz and 200Hz respectively. The amplitude of the square waveforms is 5V peak to peak. The single reference circuit gives more simplicity to adjust the duty cycle by only changing the value of Rb.

Applications such as artificial nerve stimulation for Parkinson's disease and artificial pacemaker for the heart [14] can be effectively achieved by the proposed relaxation oscillator, although the safety factor **15** implantable application is not yet discussed in this paper. In future works, it is interesting to implement the proposed relaxation oscillator to an integrated circuit, so that it can provide low cost, low power, and low frequency oscillations that can be used in implantable devices [15].

Furthermore, the simulation results also confirm that the closed-loop dual comparator circuit can perform high frequency operation as well by adjusting the RC value to smaller values while considering the comparator specification. The frequency produced using LM393 is limited due to high input offset voltage, slow rise time, fall time, and propagation delay characteristics. A higher frequency of 1MHz can easily be achieved using TLV3501 with Ra = 10k\Omega and C = 22nF. This value can be reduced further to Ra = 1 Ω and C = 1 pF, producing square wave oscillation of frequency 85 MHz, which can be verified from the simulation result in Fig. 7. If the resistor Ra is removed, a

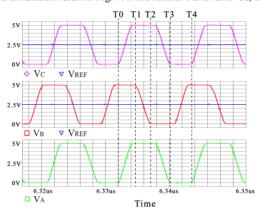


Fig. 7. A square waveform of frequency 85MHz generated using TLV3501

square waveform of frequency 86 MHz can be reached. Compared with mass product solutions like VT-803 that operates in 10–52MHz frequency band, the proposed relaxation oscillator can achieve higher frequency with more simplicity and fewer components. Relaxation oscillator using closed-loop dual comparator is a versatile solution and ideal for use in portable medical equipment, involving diagnostic imaging, ultrasound, MRI equipment, and many more [16].

IV. CONCLUSION

A relaxation oscillator using a closed-loop dual comparator for biomedical applications was presented in this paper. The proposed interconnection between two comparators was introduced to increase efficiency and lower the production cost with fewer components. The configuration of a free-running oscillator using a closed-loop

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dual comparator circuit was analyzed and formulized. The comparator circuit using 5 transistors for IC layout design was confirmed using a simulation result. The simulation and experimental results validate the proposed closed-loop dual comparator is a promising candidate for low frequency, low cost, and high efficiency relaxation oscillator. High frequency case was also simulated and cospared with mass product oscillator for medical equipment. In future works, it is interesting to design the integrated circuit of the proposed closed-loop dual comparator circuit to do further analysis and explore more about the high frequency application.

REFERENCES

- W. T. Medeiros, H. Klimach and S. Bampi, "A 40 nW 32.7 kHz CMOS Relaxation Oscillator with Comparator Offset Cancellation for Ultra-Low Power applications," 2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS), San Jose, Costa Rica, 2020, pp. 1-4, doi: 10.1109/LASCAS45839.2020.9069038.
- [2] S. Dai and J. K. Rosenstein, "A 14.4nW 122KHz dual-phase currentmode relaxation oscillator for near-zero-power sensors," 2015 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, 2015, pp. 1-4, doi: 10.1109/CICC.2015.7338396.
- [3] Y. Chang, T. Adiono, A. Hamidah and S. Liu, "An On-Chip Relaxation Oscillator With Comparator Delay Compensation," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 4, pp. 969-973, April 2019.
- [4] K. Choe, O. D. Bernal, D. Nuttman and M. Je, "A precision relaxation oscillator with a self-clocked offset-cancellation scheme for implantable biomedical SoCs," 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, San Francisco, CA, USA, 2009, pp. 402-403,403a, doi: 10.1109/ISSCC.2009.4977478.
- [5] S. Kim et al., "A low-power referenceless clock and data recovery circuit with clock-edge modulation for biomedical sensor applications," IEEE/ACM International Symposium on Low Power Electronics and Design, Fukuoka, Japan, 2011, pp. 347-350, doi: 10.1109/ISLPED.2011.5993662.

- [6] S. K. Govindan, H. Hu, C. Lin and S. Gupta, "A 25.6μW 8.97ps Period Jitter Phase-Locked Relaxation Oscillator with sub-1μS Start-Up for Low-Power IoT," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1-5, doi: 10.1109/ISCAS.2019.8702631.
- [7] H. Jiang, P. P. Wang, P. P. Mercier and D. A. Hall, "A 0.4-V 0.93nW/kHz Relaxation Oscillator Exploiting Comparator Temperature-Dependent Delay to Achieve 94-ppm/°C Stability," in IEEE Journal of Solid-State Circuits, vol. 53, no. 10, pp. 3004-3011, Oct. 2018, doi: 10.1109/JSSC.2018.2859834.
- [8] S. Kar and W. D. Leon-Salas, "A low-power 12-bit capacitance-todigital converter for capacitive MEMS pressure sensor," SENSORS, 2011 IEEE, Limerick, Ireland, 2011, pp. 1855-1858, doi: 10.1109/ICSENS.2011.6127282.
- [9] Texas Instrument. xx555 Precision Timers Datasheet. Accessed: June 2020. [Online]. Available: http://www.ti.com/lit/ds/symlink/ne555.pdf.
- [10] G. K. Kostopoulos, "Design and analysis nomograms for pulsewidth and frequency modulation using the 555 timer," IEEE Circuits Syst. Mag., vol. 6, no. 2, pp. 4–11, Jun. 1984.
- [11] H. R. Camenzind and R. B. Kash, "A low-voltage IC timer," IEEE J.Solid-State Circuits, vol. 13, no. 6, pp. 847–852, Dec. 1978
- [12] F. Everest, "The characteristics and use of the 555 timer," Electron. Educ., vol. 2000, no. 3, pp. 34–40, 2000. doi: 10.1049/ee.2000.0051
- [13] "Oral History Hans Camenzind Historic 555 Integrated Circuit Page6." 2021. Semiconductomuseum.com. 2021. http://www.semiconductomuseum.com/Transistors/LectureHall/Cam enzind/Camenzind_Page6.htm.
- [14] B. T. Anjanakumari, C. M. Bhoomika, A. A. Jugale and M. R. Ahmed, "Memristor based Relaxation Oscillator for Biomedical applications," 2019 3rd International Conference on Trends in Electronics and Informatics (ICOEI), 2019, pp. 1-5, doi: 10.1109/ICOEI.2019.8862738.
- [15] B. Ghafari, L. Koushaeian and F. Goodarzy, "New architecture for an ultra low power and low noise PLL for biomedical applications," 2013 IEEE Global High Tech Congress on Electronics, 2013, pp. 61-62, doi: 10.1109/GHTCE.2013.6767241.
- [16] "Oscillators for Medical Applications." 2021. Meddeviceonline.com. 2021. https://www.meddeviceonline.com/doc/oscillators-for-medicalapplications-0001.

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